Si/Ge Optical Bus Array and Binary Fan-out Hologram for Si-based Wafer-Scale Optoelectronic Interconnects

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REPORT I
(BMDO 94-014 Phase I)

Si/Ge Optical Bus Array and Binary Fan-out Hologram for Si-based Wafer-Scale Optoelectronic Interconnects

1.0 Introduction

Through wedding silicon and germanium, a high speed silicon superchip could be realized. This superchip utilize a intricate network of microscopic circuits that handles electrons and photons with equal ease. Its optical components amplify light, detect and channel microwave signals or laser radiation, and convert light to electricity or electricity to light. Its electronic transistors switch on and off rapidly enough for high-speed computation.

This superchip does not exist yet. Still, much work remains. The fulfillment of the vision of superchip on silicon requires passive waveguides with low propagation losses as active components such as phase modulators, amplitude modulators, mode converters, electrooptical switches, light-emitting diodes and photodetectors. All these need to be developed. Our Phase I research presents the effort to build a few of the pieces necessary for the superchip.

In our Phase I proposal, we proposed a drastically new optoelectronic chip module concept to optically interconnect Si-based VLSI wafer-scale integrated circuits. Si/Ge based optical clock signal distribution networks are promised to be developed for high speed wafer-scale integrated circuits. The key components involved are low loss channel waveguides, waveguide coupler, binary fanout holograms, and substrate waveguiding holograms. The bus architecture proposed herein represents one of the major mile stones for the realization of Si/Ge based optical bus array.

In this report, we present the demonstration of an innovative optoelectronic system using two Si/Ge wafers, where the optical bus array in conjunction with binary fan-out holograms are employed to transmit high speed optical signal at both intra- and inter-wafer

levels. This optoelectronic system employs a superstrate Si/Ge wafer due to the fact that the real estate of the Si wafer is already occupied by high packaging density transistors and logic gates. Broadcasting of clock signal requires another physical layer through which optical signal can be fanned out as required. The transparent property of Si/Ge wafer (0.5 dB/cm) allow the optical signals being distributed through the substrate waveguide based on total internal reflection. The distributed optical signal can be detected by the photodetectors fabricated on the Si/Ge substrate with high concentration of Ge. Note that the bandgap varies with Ge concentration in Si/Ge substrate. The employment of binary optical hologram provide bi-directional signals between the senders (e. g. process) and receivers (e. g. memory) in same and different wafer. More importantly, all optical components can be designed and fabricated on the same surface of the substrate, providing the possibility of using same (planar) VLSI fabrication technologies for making the integrated optical devices.

Some key components include substrate-guiding optical bus, surface-normal optical holograms, and computer simulation of the Si/Ge based optical waveguide fanout networks have been investigated in the first two months. Design and fabrication details together with experimental demonstration are reported herein.

2.0 Phase I Objectives and Project Tasks

The proposed Phase I objectives are:

Objective 1 To optimize the Si/Ge epitaxial layer thickness such that a waveguide with lowest loss will be generated,

Objective 2 To demonstrate a Si/Ge based planar fanout hologram which will provide the required optical clock signal distribution,

Objective 3 To optimize the final packaging design including lasers and detectors for Phase II Si wafer scale optical clock signal distribution,

Objective 4 To investigate and then to provide market information that projects the product development.

To fulfill the program objectives within six month time frame, the program tasks are described as follows:

Task 1	Si/Ge epitexial layer characterization.
Task 2	Si/Ge based optical bus structure simulation,
Task 3	Design of computer generated fanout hologram on Si substrate,
Task 4	Si/Ge Based optical bus fabrication,
Task 5	Si/Ge based fanout hologram fabrication,
Task 6	Device Evaluation and integration,
Task 7	Reporting.

This report details the research progress in the design of Si/Ge optical bus (Task 2), the design of fanout hologram (Task 3) and fanout hologram fabrication (Task 5). Future progress (Task 1, Task 4, and 6) will be reported in our second report in the end of January, 1995. The rearrangement in performance schedule of the seven promised tasks is due to the deliver delay of the Si/Ge wafers, which have been grown at the Lawrence Semiconductor Research Labs through subcontract arrangement. **We expect to complete this Phase I project within the six month time frame, and deliver a final report containing all the technical details and the market information needed for the continuation of this program into Phase II.**

3.0 Technical Details of The divided Tasks

3.1. Si/Ge epitexial layer characterization (Task 1)

Silicon is a promising candidate for bringing together optical, electronic, and optoelectronic circuits by monolithic integration[1-2]. It is the overwhelmingly dominated material in semiconductor electronics. This well established material can be grown on an industrial scale into nearly perfect, ultra pure crystals. Silicon manufacturing technology has advanced to the point where a typical silicon wafer costs just pennies to produce.

More importantly, when Si and Ge are combined, either as alloys or in a strained-layer superlattice (SLS), the resultant material has quite different optical and electronic properties compared to either Si or Ge. Strained Si/Ge layers have proven higher carrier

mobility , workable as high-speed electronic circuits[1-2]. By changing the composition of the Si/Ge alloy, the band-gap and the refractive index can be controlled. As a result, light can be confined in the lower band-gap (higher index) material of a single Si/Ge layer on top of silicon substrate[3-10].

In order to complete the proposed Task 1, subcontract through UT, Austin has been made to fabricate the Si/Ge epitexial layer on silicon substrate. Through this subcontract, the fabrication process for Si_xGe_{1-x} epitaxial layer growth is being investigated as the parameter of layer thickness. The different composition x = 4%, x = 7% and x = 10% are chosen and predesigned on different substrate (intrinsic, n-type and p-type). The effects of Ge composition and of the thickness of Si/Ge epitexial layer on waveguide loss will also be studied to for future design and fabrication optimization. The variation of band-gap and refractive index versus Ge composition will be investigated and then reported in the second report.

In summary, Si/Ge epitexial layer with x = 4 %, x = 7 %, and x = 10 % with thickness of 3 μm, 4 μm, and 5 μm were predesigned and is being fabricated on different substrates (intrinsic, p-type, and n-type) for future investigation. The guided wave optical bus structure simulation related to Task 2 will employ these design parameters listed in Table 1.

Table 1. Si/Ge wafer to be fabricated and investigated.

x in $Si_{1-x}Ge_x$	4 %	7 %	10 %
Thickness	3, 4, 5 μm	3, 4, 5 μm	3, 4, 5 μm
Substrate	n-, p-type	n-, p-type	n-, p-type

3.2. Si/Ge based optical bus structure simulation (Task 2)

The speed and complexity of integrated circuits are increasing rapidly as integrated circuit technology advances from very large scale integrated (VLSI) circuits to ultra large scale integrated (ULSI) circuits. As the number of components per chip, the modulation

speed and the degree of integration continues to increase, electrical interconnections are facing their fundamental bottle-necks, such as speed, packaging, fan-out, and power dissipation[11-13]. Multichip module (MCM) technology is employed to provide higher clock speeds and circuits densities[14,15]. But the state-of-the-art electrical interconnection and packaging technologies still fail to provide the required clock speeds and communication distances in intra-MCM and inter-MCM hierarchies. For example, with a clock speed of 1-GHz, electrical interconnects can only provide us with ~1 cm communication distance[13].

High speed massive fan-out optical interconnects outperform electrical interconnects[11-15]. Realizing the fact that system clock speed is at least three times higher than that of processor speed, high speed optical interconnect networks are needed for clock signal distribution in wafer-scale MCMs. Wedding silicon and germanium provides a promising approach for forming optical waveguide on silicon wafer. Compositional changes in Si/Ge alloys can be used to control the band-gap of material. Consequently, light can be confined in the lower band-gap material of a layered heterostructure with higher refractive index, i.e., the Si/Ge layer grown on silicon substrate[2-10].

Si/Ge based channel waveguide arrays have been demonstrated recently on silicon wafer at very small waveguide propagation loss of ~0.5 dB/cm[7]. It is a guided wave interconnection device that is mass producible by employing standard VLSI technology.

Our goal is to construct silicon-based waveguiding devices to deliver and to fanout high speed optical clock signal in wafer-scale MCMs. Fig. 1 and Fig. 2 show the schematic diagrams of optical bus networks under investigation in our Phase I project. In Fig. 1, the optical interconnect network is based on the guided wave devices to include optical channel waveguides, curved channel waveguides, waveguide couplers, and waveguide holograms (gratings). The substrate free-space guiding over total internal reflection and 3-D surface holograms are employed in the second approach shown in Fig. 2. One of the advantages of the second approach is that the light guiding devices do not require much silicon surface real estate, which are intensively occupied by electronic components. Both approaches provide not only the intra-wafer but also the inter-wafer high speed optical interconnections beyond that can be provided through electrical interconnects[16-17].

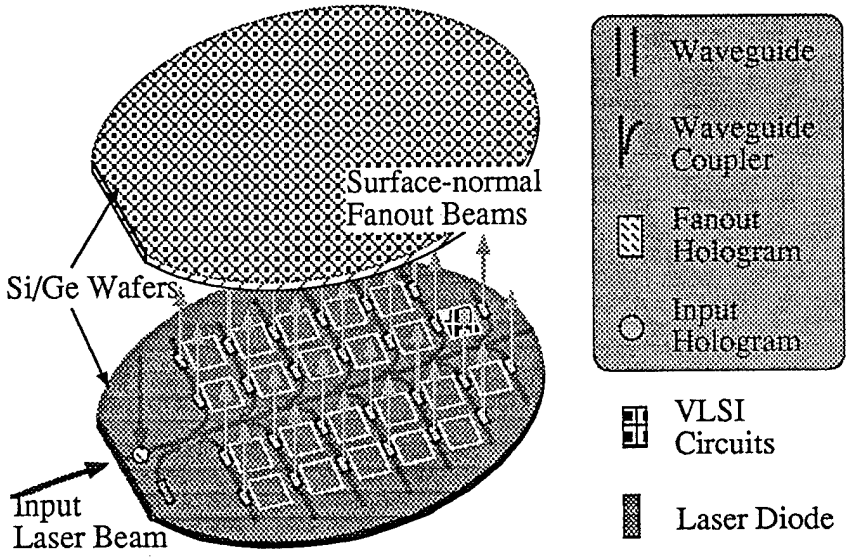


Fig. 1. Schematic of the guided wave optical interconnect for MCM clock distribution.

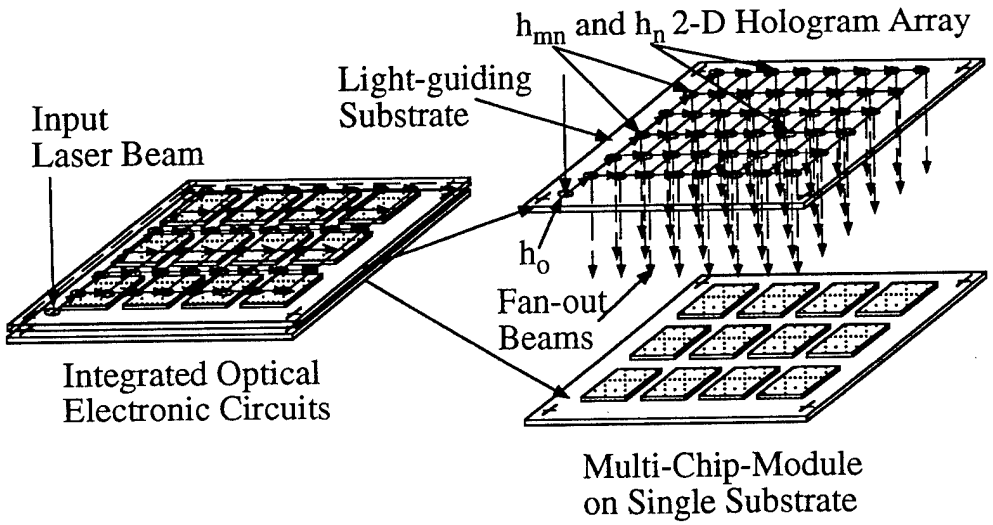


Fig. 2. Schematic of the substrate optical interconnect for MCM clock distribution.

In Fig. 1, the optical clock signal can be coupled into the channel waveguide by

(1) direct end-butt coupling from an external optic fiber, or
(2) input hologram from a laser diode mounted on another wafer (top one, e. g.),
(3) input waveguide coupler from a laser diode mounted on the wafer.

These sceranios are clearly shown in the figure. The guided optical clock signal is fanned out by an array of waveguide couplers and delivered to the desired places on the wafer. An array of surface-normal waveguide holograms are further employed to coupler the optical signal out of the waveguide. Curved waveguides are used to reduce the optical bending loss. Note that grating based perpendicular waveguide coupler are also employed in our design to avoid using curved channel waveguides. Our research will demonstrate the first integration of Si/Ge based wafer-scale optical interconnect network using waveguide devices.

In Fig. 2, The silicon superwafer itself can also function as a thin light-guiding substrate where a 2-D surface hologram array are fabricated on its surface[17,18]. The initial coupling for the optical wave is performed by a hologram (h_o) that diffract light beam into silicon substrate with diffraction angle of θ_d. θ_d is greater than the critical angle of total internal reflection, so the light is guided in the substrate through total internal reflection. As the light bounces within the silicon substrate, it encounters other holograms ($h_{m,n}$) that either re-direct it within the substrate or couple it out of the substrate surface-normally. The holograms employed have a diffraction efficiency up to 60%.

Before we experiment this idea on silicon wafer, glass substrate has been selected to study the surface hologram design and fabrication. Fig. 3 is a photograph of surface normal 1-30 highly parallel optical fanout interconnect using a glass substrate, integrated with a 2-D multiplexed hologram array. The holograms were fabricated at working wavelength of 632.8 nm, where $\eta_o = 70\%$, $\eta_{mn1} = \eta_{mn1} = 10\%$ and $\eta_n = 19\%$ were experimentally confirmed. In this photograph, a surface normal free-space HeNe laser beam (9 mW) is coupled into the glass substrate through the surface normal input hologram h_o. The parallel fan-out beams are generated by the 2-D hologram array either propagating along the substrate or normally coupling out off the substrate. The far field pattern of the 30 surface normal fan-out beams is also displayed in Fig. 3. Note that the mode dots preserve the azimuth symmetry of TEM_{oo} beam of the input laser. As a result, coupling to a 2-D photodetector array will be much easier when compared with the conventional single-mode guided wave devices.

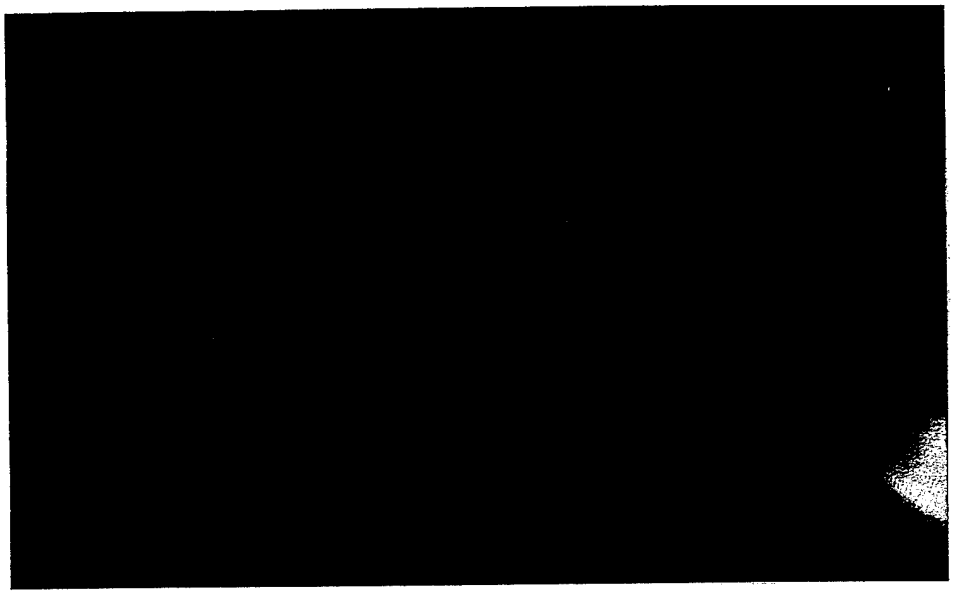


Fig. 3. Photograph of a surface-normal 1-to-30 optical fanout interconnects. The far field pattern of fanout beams is also shown.

A 25 GHz clock signal was generated using optical heterodyne technique[5], which provides equivalent modulation transfer function as that of direct modulation of a laser diode. The clock skew is minimized due to the high group velocity of the signal carrier. For a computing system with 1 GHz clock rate, this result covers up to the 25th harmonics of the fundamental frequency. Fig. 4 shows a beat signal equivalent to an optical wave modulated at a microwave frequency of 25-GHz, detected at the output of the weakest fan-out beam. A signal-to-noise ratio of 10 dB is observed.

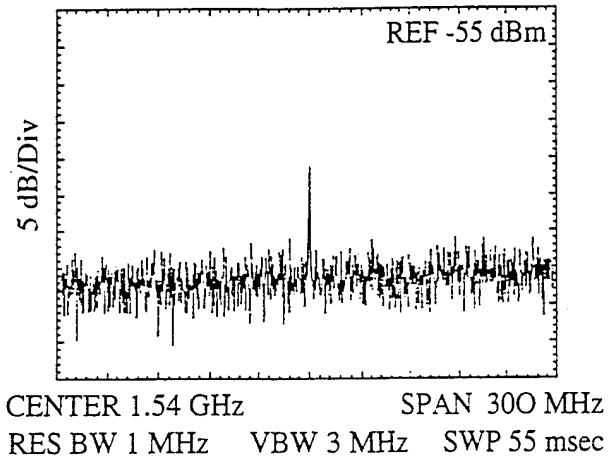


Fig. 4. 25 GHz optical beating signal through the optical interconnect shown in Fig. 3.

3.2.1. Si/Ge based optical waveguide simulation

Since our channel waveguide is made out of planar waveguide, we start our analysis with the fundamental geometry shown in Fig. 5(a). A rib channel waveguide in Fig. 5(b) and a waveguide coupler in Fig. 5(c) simulated based on coupled-mode theory (planar waveguide analysis) developed by Tayor and Yariv together with Marcutili's theory[19,20].

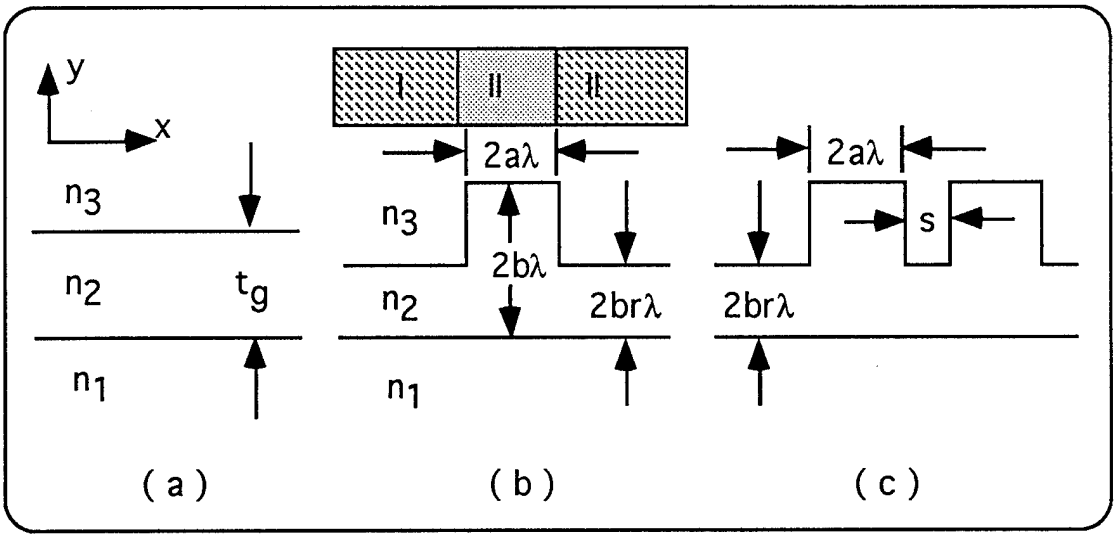


Fig. 5. Schematic diagrams of the waveguides under consideration.

Consider the three-layer waveguide structure shown in Fig. 5(a), the cladding layers with indices of refraction n_1 and n_3 are assumed to extend to infinity in the +x and -x directions, respectively. n_2 is the index of guiding layer. For the case of TE plane waves traveling in the z direction, with propagation constant β, Maxwell's wave equation reduces to

$$\nabla^2 E_y = \left(\frac{n_i}{c}\right)^2 \frac{\partial^2 E_y}{\partial t^2} \qquad (1)$$

,

with solutions of the form

$$E_y(x,z,t) = E_y(x)\, e^{\,i(\omega t - \beta z)}, \qquad (2)$$

Combing the boundary conditions, we have

$$
\begin{aligned}
E_y &= C'\exp(-qx) && (0 \le x \le \infty) \\
E_y &= C'[\cos(hx) - (q/h)\sin(hx)], && (-t_g \le x \le 0) \\
Ey &= C'[\cos(ht_g) + (q/h)\sin(ht_g)]\exp[p(x+t_g)], && (-\infty \le x \le -t_g)
\end{aligned} \qquad (3)
$$

and a transcendental equation

$$\tan(ht_g) = (p + q)/(h^2 - pq), \qquad (4)$$

where q, h and p are given by

$$
\begin{aligned}
q &= (\beta^2 - n_1^2k^2)^{1/2}, \\
h &= (n_2^2k^2 - \beta_2)^{1/2}, \\
p &= (\beta^2 - n_2^3k^2)^{1/2},
\end{aligned} \qquad (5)
$$

with $k = 2\pi/\lambda$, and $\beta = kn_{eff}$. The transcendental equation is solved numerically by a computer program we developed in phase I. Note that

$$C'_m = 2h_m \sqrt{\frac{\omega\mu}{|\beta_m|(t_g + \frac{1}{q_m} + \frac{1}{p_m})(h_m^2 + q_m^2)}}, \qquad (6)$$

m is the mode number. At cutoff condition, $\beta = kn_1 = kn_2$, the electric field becomes oscillatory in region 1 and 3. The cutoff thickness (cutt) is given by

$$cutt = \sqrt{\frac{(m\lambda)^2}{4^2(n_2^2 - n_1^2)}}, \qquad (7)$$

for symmetric waveguide, and

$$cutt = \sqrt{\frac{((2m+1)\lambda)^2}{4^2(n_2^2 - n_1^2)}}, \qquad (8)$$

for asymmetric waveguide, respectively. (Note: m = 0, 1, 2, 3, ...)

In relaxed $Si_{1-x}Ge_x$ thin film, the effective index varies with the Ge concentration and the operating wavelength. For $x < 0.25$, the linear approximation

$$n (Si_{1-x}Ge_x) = n (Si) + \delta n (x, \lambda) \qquad (9)$$

is useful, with $n \approx 3.5$ and $\delta n = 0.09x$ at a wavelength around 1.3 μm using unstrained $Si_{1-x}Ge_x$ alloy. Utilizing the Eq. (8) and Eq. (9), and $n_1 = 3.5$, $n_3 = 1.0$, we can obtain the cutoff thickness of our future waveguides as parameters of Ge concentration x. Table 2 lists our calculated results for a planar waveguide shown in Fig. 5(a).

Table 2. Cutoff thickness of planar

Ge Concentration	4 %	7 %	10 %	
Cutoff Thickness	2.1 μm	1.6 μm	1.3 μm	(1st Mode)
Cutoff Thickness	6.2 μm	4.7 μm	3.9 μm	(2nd Mode)

For channel waveguide shown in Fig. 5(b), Taylor and Yariv's theory can be employed four times (effective index method) to solve the waveguide simulation problem. First, treat region I, II and III as a planar waveguides with thickness t_1, t_2 and t_3 respectively, and calculate the effective indices n_{1eff}, n_{2eff} and n_{3eff} (of the fundamental mode). Secondly, consider region I, II, and III together as a planar waveguide with thickness of w, and index of n_{1eff}, n_{2eff} and n_{3eff} to obtain the effective index of the channel waveguide, cutoff width and electric field distribution. Based on such approach, the relation of the effective waveguide parameter for single-mode operation can be found as[21],

$$\frac{a}{b} = \left(\frac{q + 4\pi b}{4\pi b}\right) \frac{1 + 0.3\sqrt{\left(\frac{q + 4\pi b}{q + 4\pi r b}\right)^2 - 1}}{\sqrt{\left(\frac{q + 4\pi b}{q + 4\pi r b}\right)^2 - 1}} \qquad (10)$$

where r is the fraction height of the side regions compared to the rib center (the outer-to-inner ratio). The $2a\lambda$ is designated as rib width and $2b\lambda$ is the inner rib height and λ is the free-space optical wavelength. And, In Eq. (10),

$$q = \frac{\gamma_o}{\sqrt{n_1^2 - n_0^2}} + \frac{\gamma_2}{\sqrt{n_1^2 - n_2^2}} \qquad (11)$$

$\gamma_{0,2} = 1$ for TE modes and $\gamma_{0,2} = (n_{0,2}/n_{01})^2$ for TM modes.

Single-mode waveguide is interesting to us due to its small waveguide modal dispersion and its small waveguide dimension. A practical interconnect network on silicon wafer should not require large surface real estate which has already intensively occupied by electronic devices such as logic gate and high density memory. Besides, the Si/Ge based single-mode waveguides have the dimensions close to those of standard optical single-mode fibers.

Based on Eq. (9) and (10), the waveguide width for a single-mode rib waveguide is simulated as a function of Ge concentration (x), as a parameter of inner rib height. Fig. 6 shows the simulation results. If the outer-inner ratio (the fractional height of the side regions compared to the rib center) is selected to be 0.6, the rib waveguide width 5 μm can be selected for single-mode operation with SiGe thin layers at thickness of 3 μm, 4 μm and 5 μm.

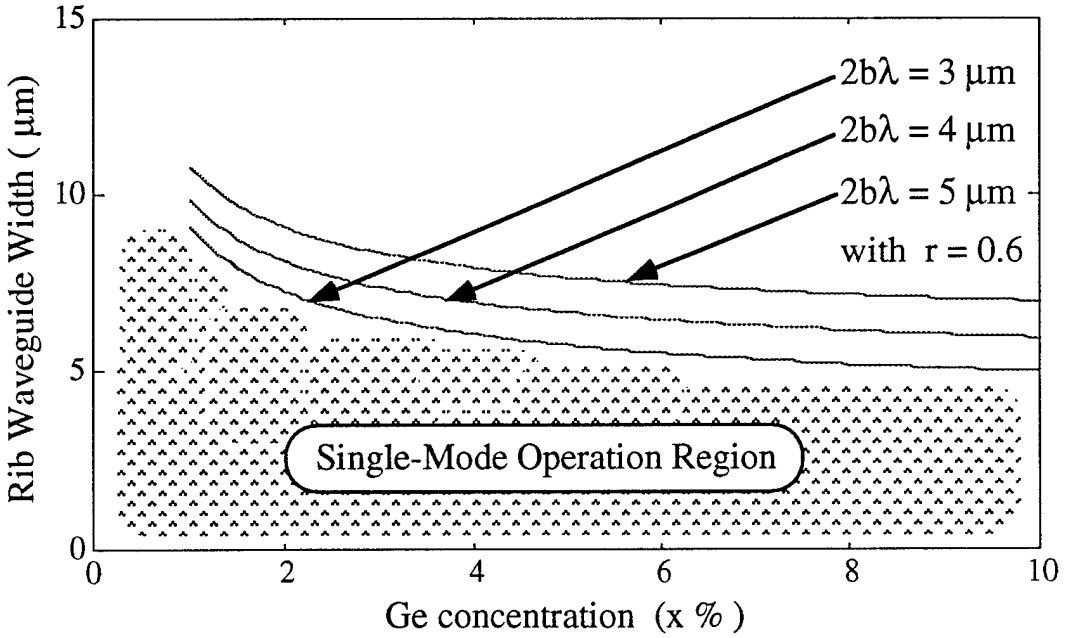


Fig. 6. Maximum waveguide width versus Ge concentration for single-mode operation.

After the waveguide width and the thickness of Si/Ge thin layer are selected, the single-mode operation depends upon the etching depth (outer-inner ration) during waveguide fabrication. Fig. 7 shows the relation between the rib waveguide width and the etching depth as parameters of Ge concentration and the thickness of the SiGe thin layer. It serves as the guiding tool to etch the Si/Ge based rib waveguide.

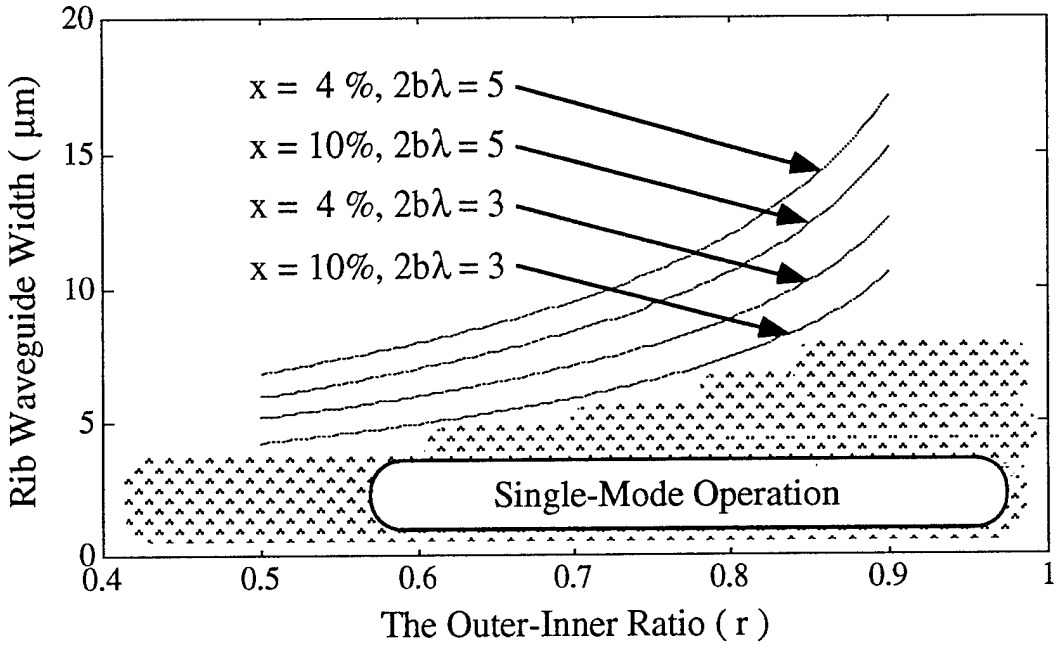


Fig. 7. Maximum waveguide width versus outer-inner ratio for single-mode operation.

Fig. 8 is the electrical field distribution in a Si/Ge based rib channel waveguide. As it indicated, the light is primarily confined in the waveguide region and silicon substrate. In the simulation, waveguide width and thickness are assumed to be 5 μm, x = 10%, r = 0.8, operated at wavelength of 1.3 μm. The disign criterion for Si/Ge waveguide bus dimension shall abide by the theoretical result presented in this section. The single-mode waveguide simulation presented here provide us the highest packing density can be achieved.

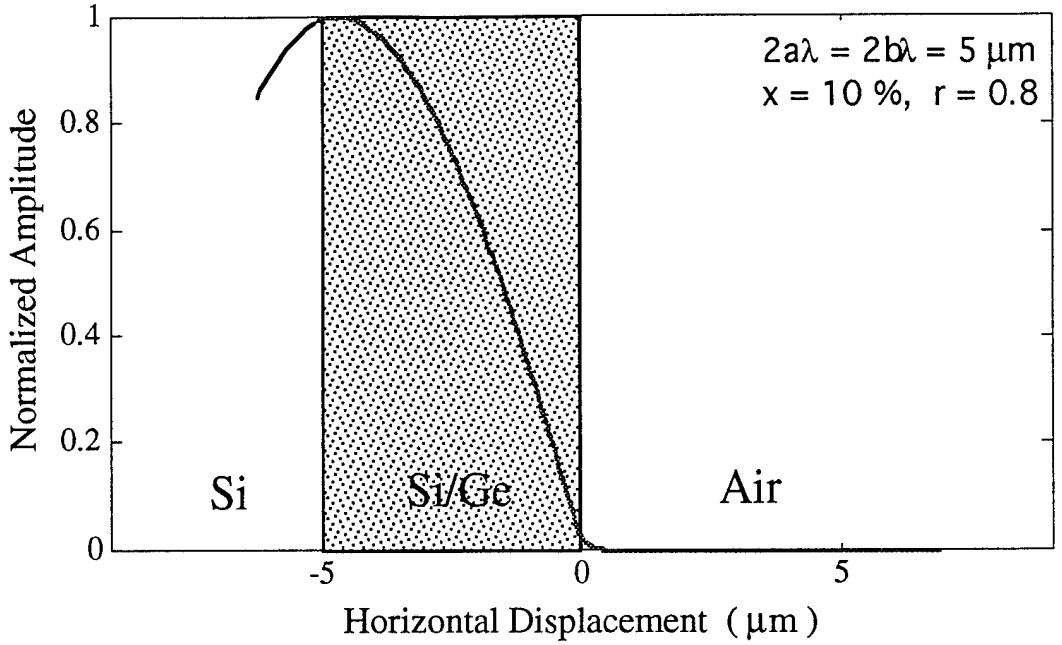


Fig. 8. Electrical field distribution in a Si/Ge based rib channel waveguide.

3.2.2 Si/Ge based waveguide coupler simulation

The schematic diagram of the waveguide coupler is shown in Fig. 5(c), which is two rib waveguides formed very close to each other. In general, a linear channel waveguide array having an infinite number of guides, the complex field in the n-th channel obeys the equation[22, 23]

$$\frac{E_n(z)}{dz} = -i\kappa E_{n-1}(z) - i\kappa E_{n+1}(z) - \frac{\alpha}{2} E_n(z), \qquad n = 0, \pm 1, \pm 2, \ldots \qquad (12)$$

where n represents the n-th channel waveguide, α is a single waveguide absorption coefficient, z is the length of channel waveguide array and κ is the coupling coefficient between two adjacent waveguides.

The coupling coefficient κ between the two waveguides is[20]

$$\kappa = 2\frac{k_x^2}{k_z}\frac{\xi_5}{a}\frac{\exp(-s/\xi_5)}{1+k_x^2\xi_5^2}, \quad \text{where} \qquad (13\text{-}1)$$

$$k_x = \frac{p\pi}{a}\left(1+\frac{A_3+A_5}{\pi a}\right)^{-1}, \quad \text{and} \qquad (13\text{-}2)$$

$$k_z = \left[k_1^2 - \left(\frac{p\pi}{a}\right)^2\left(1+\frac{A_3+A_5}{\pi a}\right)^{-2} - \left(\frac{q\pi}{b}\right)^2\left(1+\frac{n_2^2A_2+n_4^2A_4}{\pi a}\right)^{-2}\right]^{1/2}. \qquad (13\text{-}3)$$

In above equations, (13-1) to (13-3), λ is the operating wavelength, s is the channel separation, and ξ_5 represents the penetration depth of the field components in the waveguide side region. ξ_5 is given by

$$\xi_5 = \frac{A_5}{\pi}\left[1-\left(\frac{pA_3}{a}\frac{1}{1+\frac{A_3+A_5}{\pi a}}\right)^2\right]^{-1/2}, \qquad (14)$$

where $A_{3,5} = \frac{\lambda}{2}\left(n_1^2 - n_{3,5}^2\right)^{-0.5}$.

If there are only two channel waveguides (named m and n) involved in a waveguide coupler, and a power P_o is initially coupled into b at z = 0, based on Eq. (12), the interguide distribution for z > 0 is given by

$$P_m = P_o\frac{4\kappa^2}{4\kappa^2+\Delta^2}\sin^2\left[\frac{z\sqrt{4\kappa^2+\Delta^2}}{2}\right], \qquad (15)$$

$$P_n = P_o\{\frac{\Delta^2}{4\kappa^2+\Delta^2} + \frac{4\kappa^2}{4\kappa^2+\Delta^2}\cos^2[\frac{z\sqrt{4\kappa^2+\Delta^2}}{2}]\} \quad . \qquad (16)$$

Fig. 9 is a simulated result of coupling power P_a versus coupling length z for waveguide parameters $2a\lambda = 5\ \mu m$, $2b\lambda = 5\ \mu m$, x = 10 %, $s = 1\ \mu m$, and r = 0.8, based on Eq. (13-15) and effective index method. $2a\lambda$, $2b\lambda$, s, and r are defined in Fig. 5(c). x is the Ge concentation in $Si_{1-x}Ge_x$. As indicated by Fig. 9, the coupling power can be controlled by simply varying the coupling length. This is important for uniform fanout using cascaded waveguide array shown in Fig. 1. Note that the coupling length should be selected small enough to avoid the power oscillation between two waveguide.

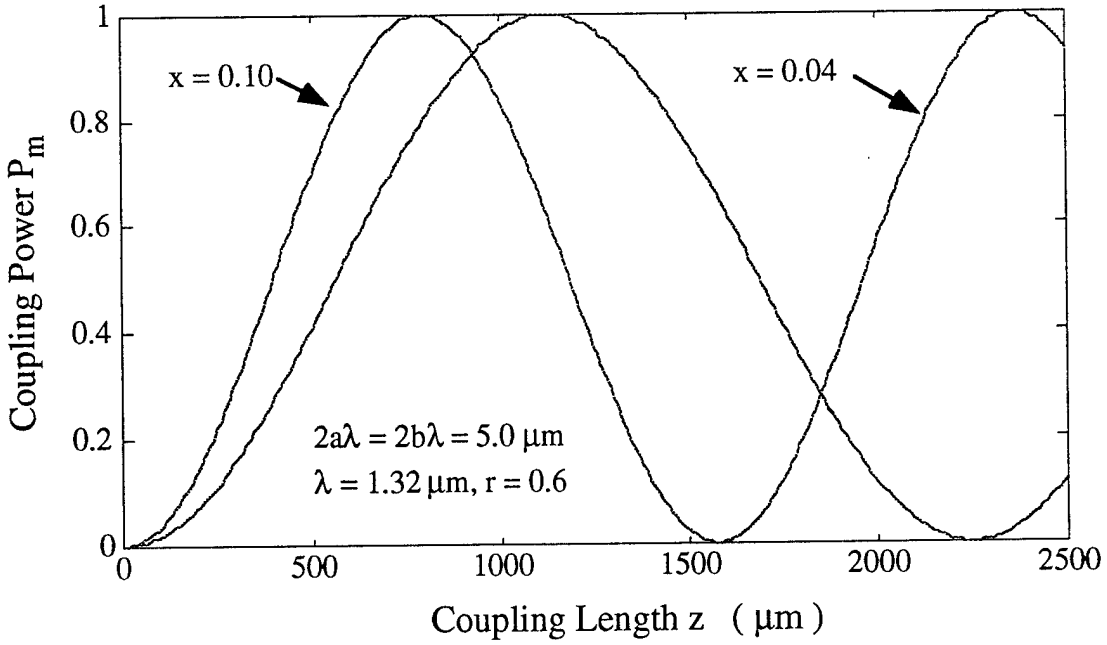


Fig. 9. Coupling power P_m versus coupling length for x = 4 % and x = 10%.

If we define the coupling ratio at the n-th fanout stage is x_n, the corresponding coupling power P_{an} is

$$P_{a1} = P_o\, x_1$$
$$P_{a2} = P_o\,(1-x_1)x_2$$
$$P_{a3} = P_o\,(1-x_1)(1-x_2)x_3$$
$$\cdots\cdots$$
$$P_{an} = P_o\,(1-x_1)(1-x_2)(1-x_3)\ldots.(1-x_{n-1})x_n \qquad (17)$$

By increasing the coupling ratio a factor of k at each stage, i.e.,

$$x_n = k^{(n-1)}x_1, \qquad (18)$$

uniform fanout can be obtained at each fanout stage. For example, in a five-stage waveguide coupler fanout array (to be shown in Fig. 11), with $P_0 = 1$, $k = 1.19$, $x_1 = 10$ %, uniform fanout in each stage can be obtained, and listed in Table 3.

Table 3. Fanout Power in a Cascaded Five-Stage Waveguide Coupler Array

Fanout Stage	1	2	3	4	5
P_{an}	0.10	0.11	0.11	0.11	0.10
z	230 μm	253 μm	274 μm	299 μm	332 μm

Due to the concerns of SiGe thin layer fabrication and waveguide dimension, different thickness of the SiGe thin layer were selected and are currently in fabrication in this research project. Through controlling the etching depth, same waveguide width in the waveguide coupler array can be used to provide equal performance. In other wards, same design mask can be used to fabricate the waveguide network based on different $Si_{1-x}Ge_x$ epitaxial layers with different thickness and Ge concentration. Fig. 10 shows simulated results of the coupling power versus coupling length for a five-stage cascaded waveguide coupler fanout array, using two different $Si_{1-x}Ge_x$ epitaxial layers (x = 4 % and x = 10 %) with two different thickness as 3 μm and 5 μm. Channel separation is 1 μm in the waveguide coupler.

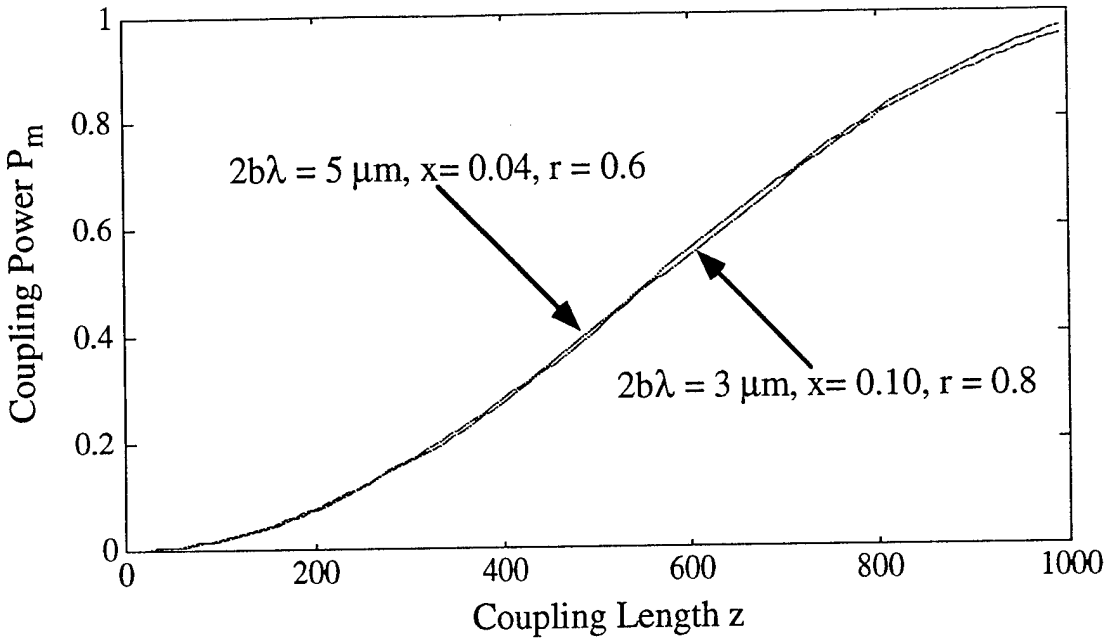


Fig. 10. Coupling power versus coupling length for two waveguide couplers. Same waveguide width and different epitaxial layers and layer thickness are assumed.

Another important concern is the radius of curved waveguide to be employed in our design. To avoid waveguide bending loss, a minimum radius of curvature has to be known during the design, which is a complicated function of the waveguide parameters. It has been found that the loss due to waveguide bending can be negligible small[24], if

$$R > \frac{3\lambda n_{eff}^2}{\pi[n_{eff}^2 - n_c^2 + (\frac{1}{2b})^2]^{3/2}} \qquad (19)$$

where n_{eff} is the guided wave effective index, and n_c is the effective index of cladding region. The calculated minimum radii for different waveguide parameters based on Eq. (19) and effective index method are listed in Table 4.

As indicated by Table 4, the required radii of the waveguide curvature are in the range of from 5 mm to 12 mm using our waveguide parameters. Based on this result, we selected R = 12 mm in our design to avoid the significant waveguide bending loss.

Table 4. Calculated Minimum Radii of Curved Waveguides

$R_{min}R$	Waveguide Width	Waveguide Height	Outer-to-inner Ratio	Ge Concentration	Wavelength
	$2a\lambda$	$2b\lambda$	r	x	λ
5.9 mm	5 μm	3 μm	0.8	4%	1.32 μm
5.3 mm	5 μm	3 μm	0.8	10%	1.32 μm
6.0 mm	5 μm	5 μm	0.8	4%	1.32 μm
12.0 mm	5 μm	5 μm	0.9	4%	1.32 μm
6.2 mm	5 μm	5 μm	0.8	10%	1.32 μm
5.2 mm	5 μm	5 μm	0.6	10%	1.32 μm

3.2.3 Optical mask design for Si/Ge based waveguide network

Based on above simulations, optical masks, containing the channel waveguide Mach-Zehnder interferometer, waveguide ring resonator, single-mode and multimode channel waveguide array, and waveguide fanout coupler arrays as shown in Fig. 11. The single-mode waveguides have channel width of 5 μm, and multi-mode waveguides have channel width of 50 μm. Waveguide couplers have separation of 1 μm, 1.5 μm and 2 μm. Waveguide network shown in region d and f are also waveguide fanout networks, where the waveguide holograms will be future fabricated to couple the guided wave from the vertical waveguide into the horizontal waveguides. The optical mask are laid out using standard AUTOCAD and fabricated by Mask Generator. These masks will be used in achieving Task 4. And the results will be reported in the second report.

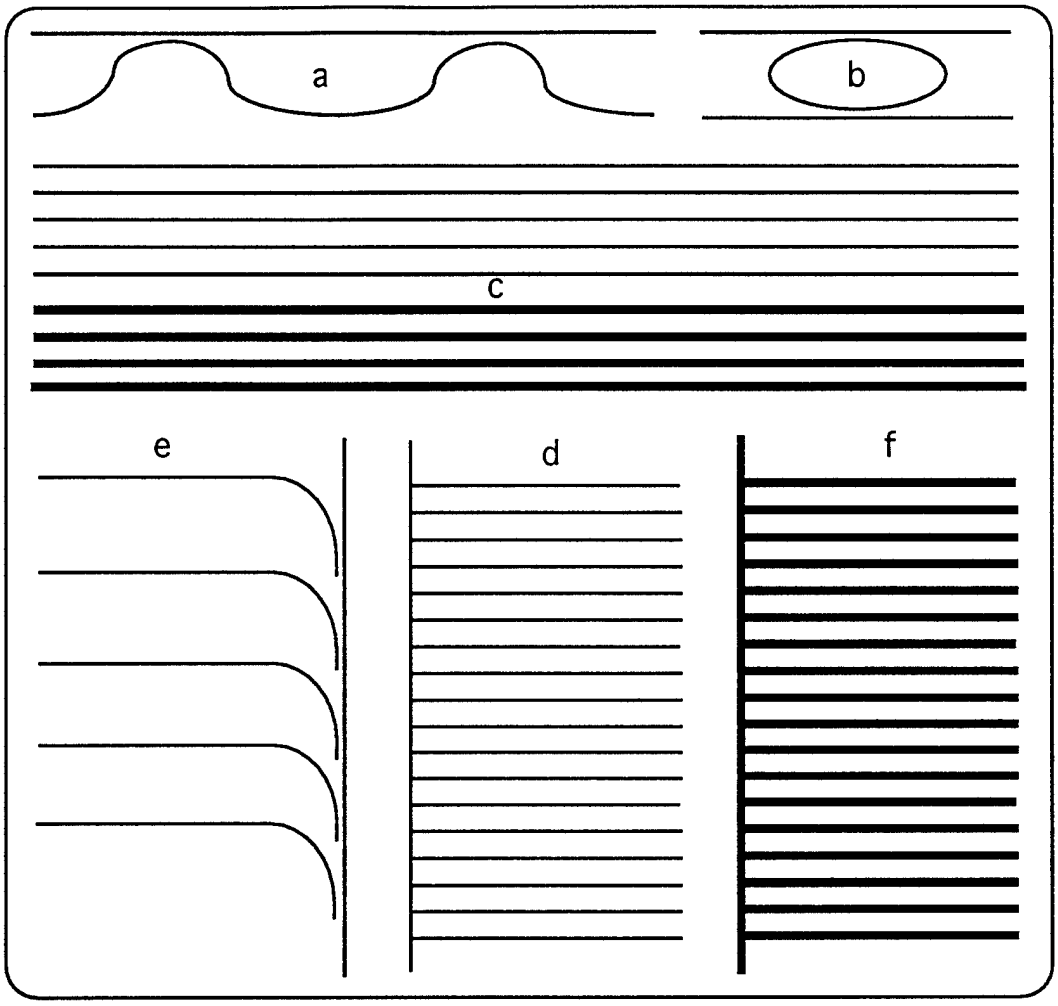


Fig. 11. Schematic diagram of the optical mask designed in Task 2.

In summary, we have build a theoretical model to provide the computer simulation, which is needed to support the fabrication condition such as waveguide thickness, width, Si/Ge ratio, separation of waveguide coupler, etching depth, and wavelength of optical signal. Based on these simulations, the Si/Ge wafer with different thickness and Ge concentration are selected. Optical masks are designed to utilize both single-mode and multi-mode waveguide array, and single-mode waveguide coupler array. The variation of etching depth to obtain single-mode operation and desired optical coupling ratio is also simulated.

3.3. Design of Computer Generated Fanout Hologram (Task 3)

Among the optical interconnect architecture demonstrated thus far, optical interconnects based on two-dimensional waveguide array and free-space interconnections represent current technology trends[25-27]. Each of these optical interconnect technologies has its own appealing properties. Waveguide-based optical interconnects are suitable for in-plane bus-connections, while free-space interconnects are suitable for board-to-board interconnections.

In this research, we investigate a unique optical interconnect scheme for highly parallel massively optical fan-out. The device proposed herein minimizes the employment of real estate of semiconductor surface. Unlike the guided wave and free-space optical interconnects, both intra- and inter-board highly parallel massive fanout can be realized, using a silicon substrate in conjunction with a 2-D array of planar holograms. The schematic diagram of the proposed optical interconnect network is shown in Fig. 2 Because all the planar holograms can be arranged in the same surface of silicon, planar technologies, developed through fabrication VLSI circuits, can be employed to fabricate the devices proposed herein. More importantly, the parallel feature among fanout beams and the planar compact device structure convert the un-solvable three spatial and three angular multiple alignment problem into a single step 2-D planar one.

3.3.1. Design of Planar Hologram on Silicon wafer

A simple form shown in Fig. 12 can be used to study the use of planar holograms on silicon substrate for optical interconnections. An optical beam carrying information or a clock signal is incident on the input hologram with normal angle of incidence and generates diffracted beams. These diffracted beams are confined within the substrate by total internal reflection (TIR). After propagating within the silicon substrate in the orthogonal direction, the TIR beam can incident on a detector or surface-normally coupled out of the substrate by another planar hologram.

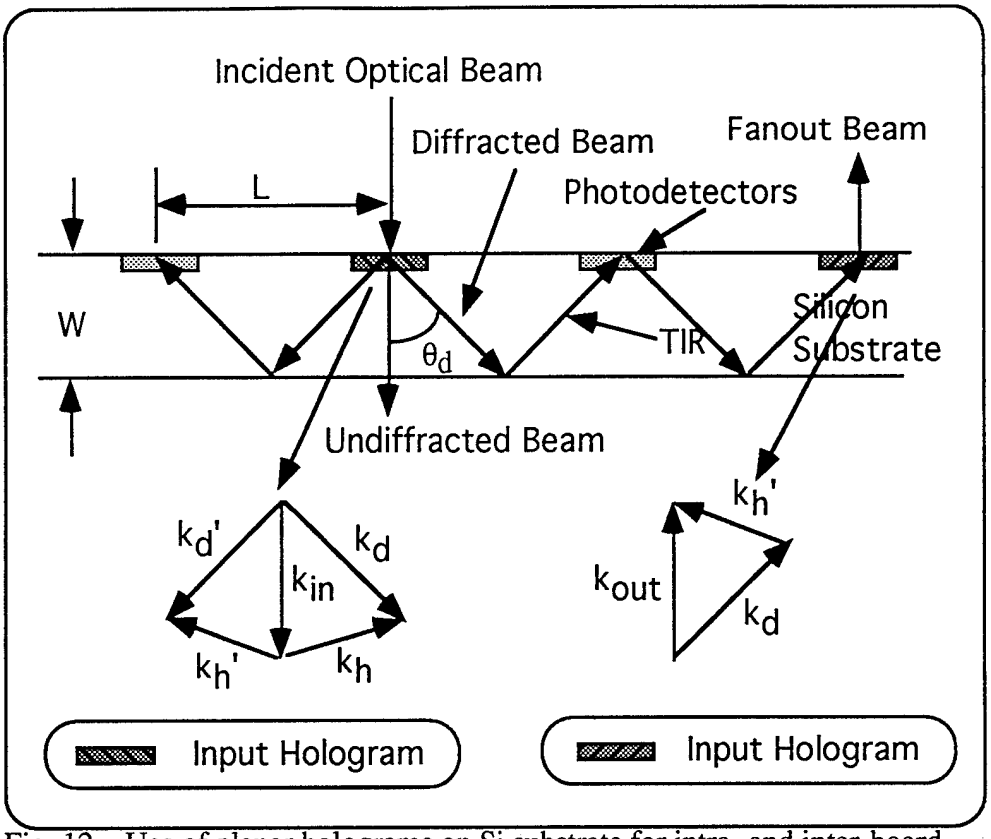


Fig. 12. Use of planar holograms on Si substrate for intra- and inter-board optical interconnects. Phase-matching diagrams are also shown.

As shown in Fig. 12, the beam is normally incident from the region with refractive index n_1, $n_1 < n_2$, $k_{h//}\Lambda = 2\pi/\Lambda$ is the grating vector in the substrate surface with period Λ, the angle between the forward diffraction order and the incident beam is

$$\mathrm{Sin}\theta_m = \frac{m\lambda}{n_2 \Lambda} , \qquad (20)$$

where m = 1, 2, 3.. is the diffraction order. The diffraction beam can be confined to the substrate by total internal reflection (TIR) if the diffraction angle θ_m is greater than the critical θ_c, given by

$$\theta_c = \mathrm{Sin}^{-1}(n_1/n_2) \qquad (21)$$

where n_1 is the index of substrate surrounding medium, and n_2 is the substrate index. Combining Eq. (21) and Eq. (20), we determined that

$$\Lambda < \frac{m\lambda}{n_1} \quad . \qquad (22)$$

On the basis of Eq. (22), the grating become increasingly more difficult to fabricate for short optical wavelength to satisfy TIR. In our case, silicon is only transparent at wavelength above 1.2 μm, longer wavelength is preferred based from the grating fabrication point of view. However, it is more difficult to make optical detector on Si/Ge wafer working at longer wavelength. 1.3 μm optical wavelength is selected as a tradeoff, This wavelength is widely employed in fiber communications. The fabrication difficulty can be somewhat relaxed for higher diffraction orders (m > 1).

In the geometry of Fig. 12, we determine the required grating period Λ as a function of diffraction angle θ_m, m, λ, n_1 and n_2, and which is

$$\Lambda = \frac{m\lambda n_1}{n_2 \tan\theta_m}[1 + \tan^2\theta_m]^{\frac{1}{2}} \quad . \qquad (23)$$

The plot of Λ as a function of θ_m for silicon substrate is shown in Fig. 13. In the plot, $n_1 = 1.0$, $n_2 = 3.5$, m = 1, λ = 1.3 μm are assumed. The plot is divided into two sections, the left one is non-TIR region, and the right one is TIR region. As indicated in Fig. 13, fine gratings with period less than ~1.3 μm are required in fabricating our proposed devices. We shall study the existing technologies for such fine device fabrication in the following.

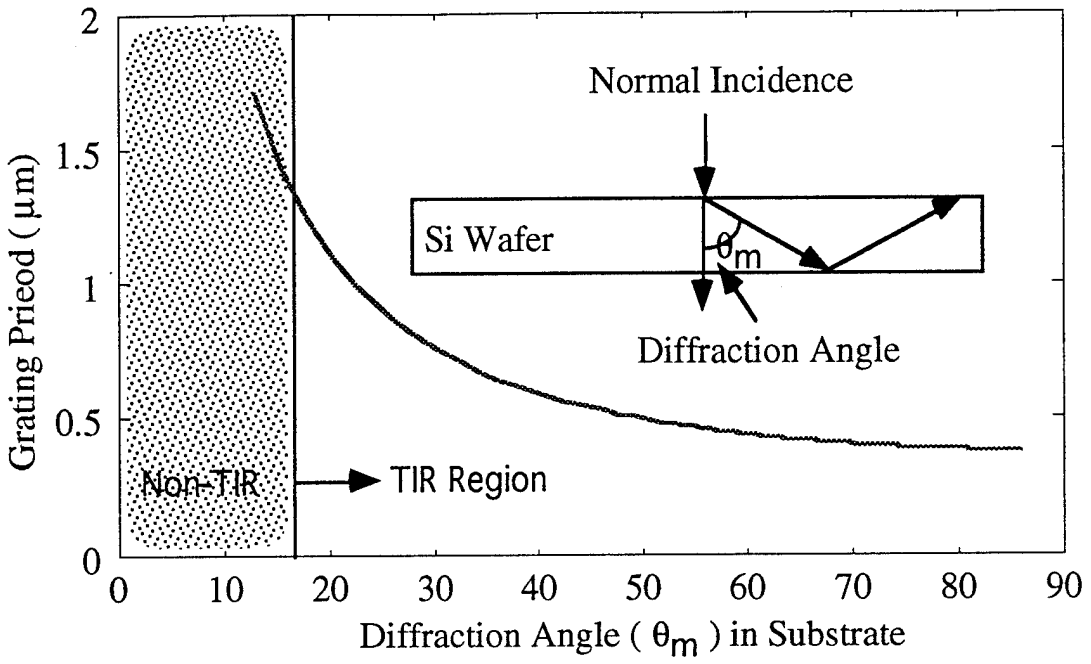


Fig. 13. Plot of grating period as a function of diffraction angle for silicon substrate.

3.3.2. Fabrication technologies for planar holograms

There are more than four different optical hologram fabrication techniques, which can be employed to make the device under investigation. They are:

a. Microlithography (with e-beam generated masks),
b. Holographic recording,
c. Laser direct writing, and
d. Laser assisted microfabrication.

Table 5 summarizes the performance features of various technologies with respect to key parameters of optical holograms fabricated. It serves as a guideline for our experimental study and will be discussed in more details below.

Table 5. Performances of the optical hologram generation technologies.

Type / Items	Micro-Lithography	Holographic Recording	Laser Direct Writing	Laser Assisted Micro Fabrication
Smallest Grating Period	0.5 μm	0.2 μm	2 μm	4 μm
Period Accuracy	0.1 μm	0.01 μm	0.1 μm	0.01 μm
Exposure Time	30 sec/cm^2	20 sec/cm^2	10 hrs/cm^2	200 hre/cm^2
Groove Profile Control	Staircase Approxi-mation	Smooth Sinusoidal Like Profile	Full Control	Good Control Possible
Diffraction Efficiency	8 Levels < 95%	> 80%	> 95%	High Efficiency Possible
Cost	Low Cost Possible	Low Cost Possible	High	Very high
Remarks	Ideal for Complex Patterns	Ideal for High Spatial Frequency	Ideal for Complex Patterns	Promising for Integ. Optics

(a). Microlithography With E-Beam Generated Masks

With microlithography we can fabricate optical holograms in mass scale and consequently at a low prize. However, if we have to deal with multilevel structures for high diffraction efficiency, the microlithography process becomes tedious and alignment errors of the masks lower substantially the production yield of such components[28]. Various design software tolls have developed[29-32], to employ computer for generating binary pattern, and then translate into appropriate formatting for E-beam mask generators.

(b). Holographic Recording

Often there is nothing like the "classical holographic technology" to produce the desired optical holographic devices[17,33]. This technology is the only one presently that can provide very small grating period down to about 0.2 μm on large surface. Also, the value of the groove period can be controlled to the order of 0.01 μm simply by controlling

the angle between the two interfering laser beams. This precision on the groove period is at least one order of magnitude better than the other technologies. Finally, holographic recording provides naturally smooth surface relief structures as compared to sharp edges of binary structures. This last feature is highly desirable when the devices is to be used with high peak power lasers as it is the case for the holographic beam sampler[34]. In our experiments, we employ holographic recording technique mainly based on its short exposure time, which speed up our research.

(c). Laser Direct Writing

Laser direct writing, one of the laser induced fabrication methods, employs a scanned micrometer or sub micrometer reaction for serial, real-time machining of the workpiece. Laser direct writing technique is able to produce gratings in photoresist with well controlled groove profile. Good linearity of the photoresist thickness versus the laser energy dose can be achieved. The laser written pattern can always be transferred to other optical substrate with standard etching equipment. Best of all, two dimensional holographic components with continuos groove profile can be fabricated[35].

(d). Laser Assisted Microfabrication

Vigorous research activity has been directed over the last few years to laser processing for microfabrication. The new technique is motivated by the proven feasibility ranging from the achievement of submicron feature size to development of laser direct writing methods for various applications in IC manufacturing and prototyping in optical waveguide and hologram fabrication. Laser induced microfabrication technology utilizes the laser-controlled microchemical reactions leading to deposition, etching and doping of various materials. The methods for deposition, etching, and doping of different materials are at this point already based on several hundred different surface reactions[36]. In these well controlled photochemical or thermal reactions in vapors or liquids, a line width of 0.2 μm, well below the diffraction limited laser spot size, can be achieved even with visible light. This technique offers flexibility not achievable with the standard patterning methods and may be quite suitable for prototyping and even manufacturing of short series of custom structures and devices, specially if one considers continuous groove profile.

In this research, both technologies using holographic recording and microlithography with e-beam generated masks will be investigated for the surface hologram fabrication. Holographic recording is chosen based on its capability of providing smallest grating period (0.2 μm) and short processing time at very low cost. The microlithography

technique is also selected simply because it is a standard VLSI fabrication technology. It certainly provides the possibility of creating electronic and optic circuits in the same substrate (such as silicon) using same fabrication technologies.

3.4 Si/Ge Based Optical Bus Fabrication (Task 4)

All optic elements including holographic gratings are arranged in the same surface as shown in Fig. 2 and Fig. 12. Holographic recording and standard VLSI fabrication technology will be employed for device fabrication. One of our research goals is to create electronic and optic circuits in the same substrate (such as silicon) using same fabrication technologies.

The proposed fabrication of our optical bus array is based on selective chemical etching on silicon substrate, to generate surface-relief holographic gratings. This silicon etching process was original developed in semiconductor integrated circuit industry in forming the surface-relief structure in VLSI circuits. In brief, this process involve light exposures on the photoresist material spin-coated on the surface of substrate. The desired holographic grating pattern can be generated by conducting the light exposure through imaging a designed mask, where the grating period and the location of the gratings are arranged as designed. The desired grating pattern can be also produced through directly optical holographic writing and/or mask imaging, which are all commonly employed in VLSI fabrications. A microcrystallined phase is produced in the light exposed region of the photoresist material. This crystallization leads to a stronger (or weaker) chemical resistance during the followed chemical etching process. As the results, the surface-relief grating can be formed on the surface of substrate by the selective chemical etching.

Fig. 14 illustrates the photolithographic process of grating fabrication. The are three steps involved in this processes. They are

(1) spin-coating a selected photoresist on the desired substrate surface;
(2) writing the desired gratings pattern onto the photoresist layer;
(3) chemical-etching to generate the surface-relief gratings.

During this Phase I program, the most suitable method for grating pattern generation onto the photoresist will be determined to provide high quality grating for our optical bus array.

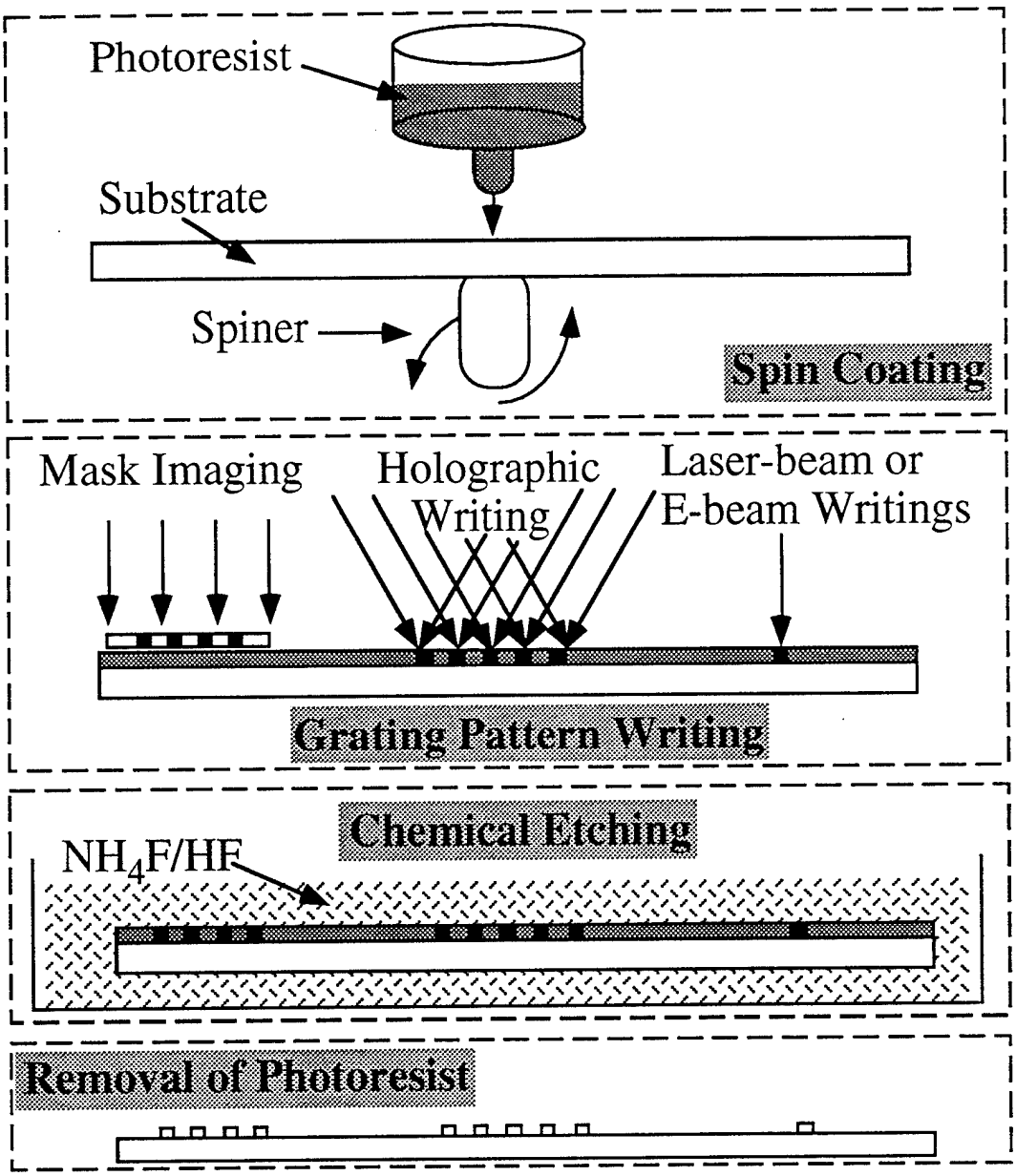
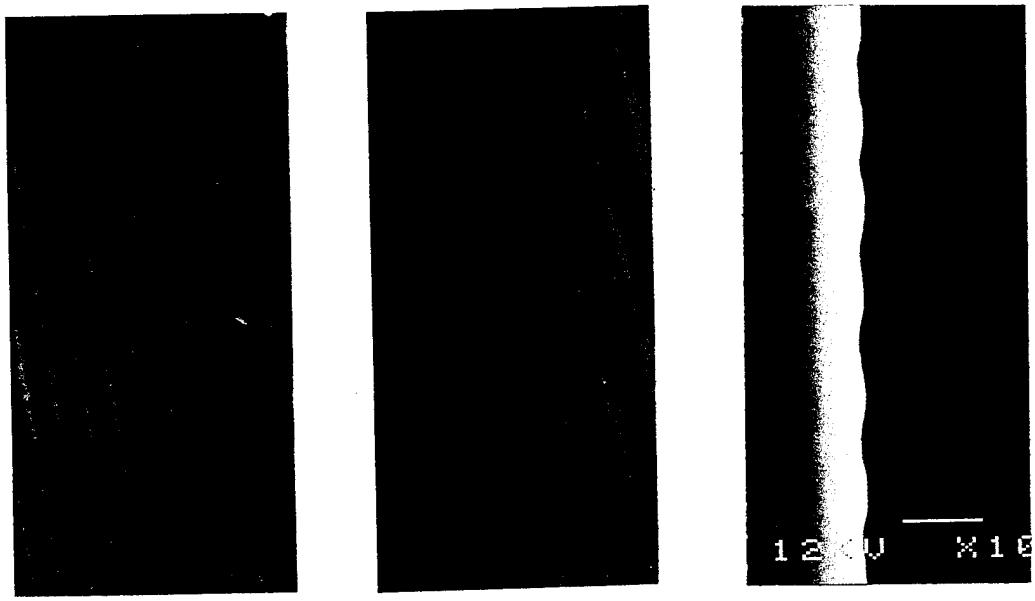


Fig. 14. Photolithographic process of holographic grating fabrication.

In the first two months of this Phase I project, we has fabricated holographic phase grating on glass substrate as shown in Fig. 15(a), and surface-relief gratings on silicon substrate as shown in Fig. 15(b). The diffraction efficiency was adjustable up to 70% using holographic thin film on glass substrate. Because the crystallized structure of silicon, surface-relief through chemical etching follow the crystal lattice plane as indicated in Fig. 15(b). Fig. 15(c) is the transverse micropicture of the silicon surface-relief grating fabricated.



(a) (b) (c)

Fig. 15. Fabricated holographic gratings on (a) glass, (b) silicon substrate. Fig. 5(c) is the transverse micropicture of silicon grating fabricated.

The diffraction efficiency of the surface-relief grating can be controlled by (1) varying the grating depth, (2) varying grating width, and (3) varying grating shape[29]. These three possible approaches are schematically shown in Fig. 16. All these three techniques will be investigated in this Phase I project. A physical modal for calculating the diffraction efficiency of silicon surface-relief grating will be developed at the end of Phase I project.

To fabricate an optical bus using substrate guiding as shown in Fig. 12, a double side polished silicon wafer is employed as a light guiding plate. Two surface holograms are fabricated, serving as an input hologram and an output hologram, respectively. The optical beam is coupled into an silicon substrate by the input hologram, and then propagates within the silicon substrate. The diffraction angle is designed at 45 degree working at 1.32 μm. The substrate guided beam is transmitted over 2 cm and coupled out of the substrate by the output grating. Fig. 17 is the photograph of the device demonstrated in our research. The optical beam is provided by a YAG laser of wavelength 1.32 μm.

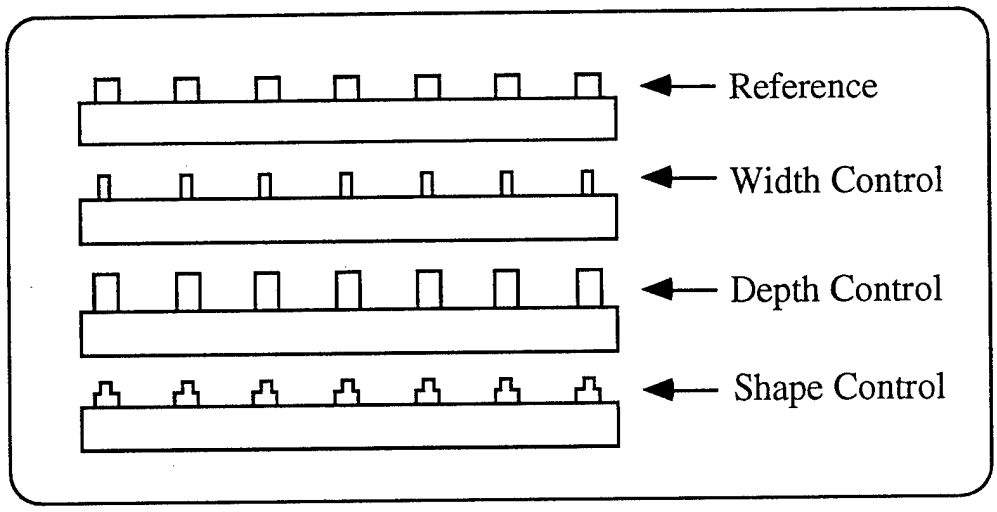


Fig. 16. Techniques for diffraction efficiency control for surface-relief grating.

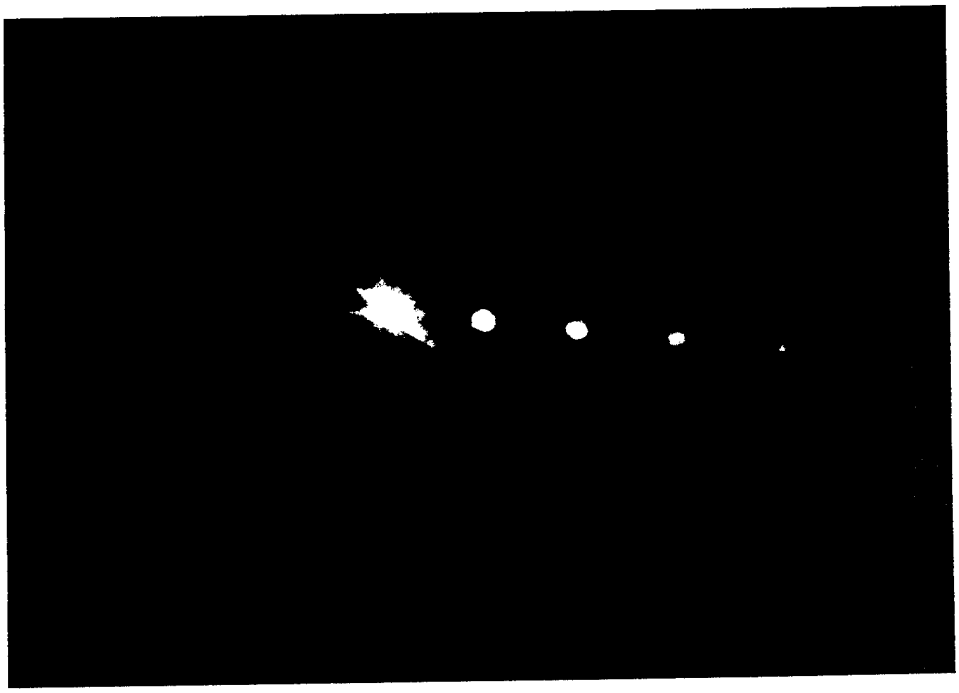


Fig. 17. Photograph of a silicon substrate guided optical interconnect.

The hologram recording setup used for the device fabrication is shown in Fig. 18. A powerful Ar^+ laser with output power up to 10 W is employed to record the hologram. The laser is operated in single wavelength (456 nm, 488 nm or 514.5 nm). The 20X micro

objective lens is used to expand the laser beam, followed by a spatial filter located at its focal point. The plane wave is formed by employing another large diameter reflection lens. Part of the incident plane wave serves as the recording beam while another part of the plane is reflected by a mirror, serving as the reference beam. Both the recording plate and the mirror are mounted on two three spatial microtranslation stages and three angular rotation stages, respectively, with resolution of 0.2 μm and 0.05° degree, respectively. As a result, the incident angles (θ_1 and θ_2) of the two recording beams, which determine the grating period generated, can be well controlled during the recording.

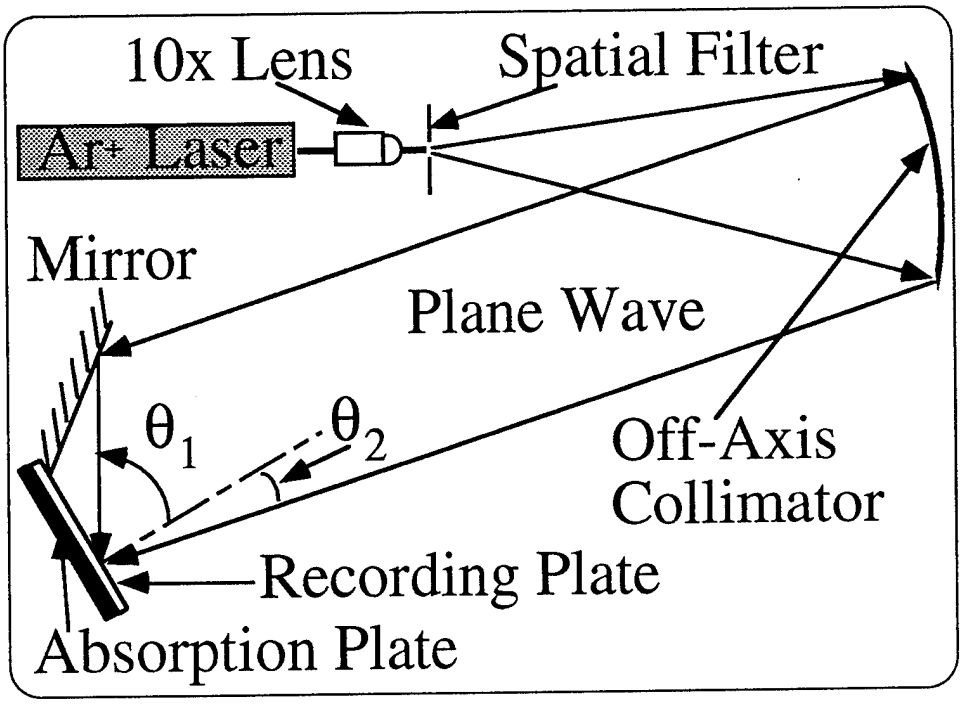


Figure: 18. Schematic diagram of hologram recording setup.

A absorption plate with index match to the index of recording substrate is found to be very useful to reduce the back side reflection during the hologram recording. Further experimental results will be provided in the next bi-monthly report.

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